REMARKS

Interview Summary

Applicant's representative wishes to thank Examiner Farahani for the courtesies extended during the interview of April 19, 2007. During the interview, the merits of the rejections were discussed, including remarks regarding the failure of the references to disclose selectively depositing an oxide, as claimed. Additionally, the Examiner's motivation set forth at page 3 of the Final Office action for combining the teachings of the Puchner and Cabral references was discussed. Examiner Farahani indicated that in view of the arguments the application may be allowable over the prior art references now applied, but asked that arguments be presented in writing.

Rejections under 35 USC §103

Puchner in view of Cabral

The Office has rejected claims 1, 2, 9, 10, 11, 18, 19, 24 and 25 as being unpatentable under 35 USC §103 over U.S. Patent Application No. 2003/0045062 ("Puchner") in view of U.S. Patent No. 6,921,711 ("Cabral"), for the reasons set forth at pages 2 to 3 of the Office Action. Applicants respectfully traverse this rejection.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in

the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See M.P.E.P. § 2143.

Claim 1, which reads as follows, is representative of the claims of the present application:

> A method of fabricating a semiconductor device, the method comprising:
> forming a gate on a semiconductor substrate, the gate including opposing side surfaces and a top surface;
> after forming the gate, selectively depositing an oxide material comprising at least one material from the group consisting of AlO_3, ZrO_2, HfO_2 (AlHf) O_x, HfO_2, La_2O_3, Y_2O_3, silicon oxynitride, and hafnium silicon oxynitride substantially on the top surface of the gate, as well as over the semiconductor substrate, the opposing side surfaces of the gate being substantially free of the oxide material; and
> forming spacers on the opposing side surfaces of the gate subsequent to depositing said oxide material, the spacers contacting the opposing side surfaces of the gate substantially along the opposing side surfaces.

Neither Puchner or Cabral, either taken separately or in combination, teach or suggest applicants claimed invention.

Puchner teaches an oxide layer 22 formed over a polysilicon gate layer 20. See. FIG. 2 and paragraphs [0022] and [0023]. Etching to form a gate, as illustrated in FIG. 3, is performed after the oxide layer 22 is deposited. See paragraph [0027]. The integrated circuit is exposed to a first species that primarily contacts the horizontal surfaces and preferentially does not appreciably contact the vertical surfaces. Oxide sidewalls are then grown, as shown in FIG 5.

According to the Examiner, Puchner does not disclose the oxide is one of the claimed materials, such as silicon oxynitride. See outstanding Final Office Action, page 2. To supply this teaching, the Examiner relies upon Cabrel, which discloses high-K dielectrics for use as a gate dielectric. Cabral, column 7, lines 26 to 35. As motivation

for combining the references, the Examiner has indicated that it would have been obvious to make the gate dielectric of Puchner a high-K gate dielectric, because it is well known that high K gate dielectrics protect against dielectric breakdown. The Examiner further alleges that it would have been obvious to make the top of the gate insulator the same material as the gate insulator to simplify the process, as the high-k material would have been readily available.

Applicants respectfully disagree with the proposed motivation. The Puchner and Cabral processes are entirely different processes. For example, Puchner is directed to forming a polysilicon gate, as discussed above. Cabral, on the other hand, is directed to a forming a metal gate using a sacrificial gate structure. See e.g., Cabral, Abstract, column 6, lines 35-38 and column 9, lines 24-26. Further, there is no suggestion in Cabral to support employing the same insulator on top of the gate as is used for the gate insulator, as the Examiner suggests. Given the disparate teachings of these references and the lack of any suggestion in the references to combine their teachings, there is not sufficient motivation to support a *prima facie* case of obviousness for combining the references in the manner suggested by the Examiner.

Further, even if Puchner and Cabral were combined as suggested by the Examiner, the combination would not result in the claimed method. This is because neither Puchner nor Cabral teach or suggest selectively depositing an oxide material on the top surface of the gate after forming the gate, as is recited in the present claims. Rather, as discussed above, Puchner teaches forming an oxide on a polysilicon layer and then etching the oxide and polysilicon to form the gate. Carbral does not appear to

teach an oxide layer on a top surface of the gate, and thus cannot suggest such a teaching.

Without at least some teaching or suggestion of selectively depositing the oxide, as claimed, no *prima facie* case of obviousness has been made. For at least this reason, the rejections should be withdrawn.

Regarding claims 18 and 19, these claims depend from claim 12, and thus include every limitation of claim 12. However, because claim 12 was not rejected, it is unclear how claim 18 and 19 can be rejected. Applicants request clarification from the Examiner regarding this issue.

Puchner in view of Cabral and Jin

The Office has rejected claims 8, 12 and 13 under 35 U.S.C. §103(a) as being unpatentable over Puchner in view of Cabral, as applied above, and further in view of U.S. Patent No. 6,734,108 ("Jin"), for the reasons set forth at pages 3-4 of the outstanding Final Office Action. Applicant respectfully traverses the rejection.

For the reasons discussed above, Puchner and Cabral fail to teach or suggest every element of the claimed invention. In particular, neither Puchner nor Cabral teach selectively depositing an oxide material on the top surface of the gate after forming the gate, as is recited in the present claims.

Jin does not cure the deficiencies of Puchner and Cabral. Instead, Jin teaches non-selectively depositing a gate top insulating layer 610 over a gate conducting layer 608 prior to forming a gate, as shown in FIG. 6A, and then etching both layers 610 and 608 to form a gate structure, as shown in FIG. 6B. *See also,* Jin, Column 9, lines 60-63 and column 10, lines 20-22.

Thus, the Puchner, Cabral and Jin combination fail to teach every limitation of the claims. Because every limitation of the claims is not taught, no *prima facie* case of obviousness exists, and the rejection should be withdrawn.

Puchner in view of Cabral and Jeng

The Office has rejected claims 4, 6, 14 and 15 as being unpatentable under 35 USC §103 over Puchner in view of Cabral, as applied to claims 1 and 12, and further in further in view of U.S. Patent No. 6,303,490 ("Jeng"), for the reasons set forth at page 4 of the Office Action. Applicants respectfully traverse these rejections.

As an initial matter, it is noted that claim 12 was not rejected over the Puchner and Cabral combination, as asserted above. Clarification of this issue is requested from the Examiner.

For the reasons discussed above, Puchner and Cabral fail to teach or suggest every element of the claimed invention. In particular, neither Puchner nor Cabral teach selectively depositing an oxide material on the top surface of the gate after forming the gate, as is recited in the present claims.

Jeng fails to cure the deficiencies of the Puchner and Cabral combination. Instead, Jeng teaches an anisotropic deposition process employed in a dual damascene process to form an interconnect, and does not appear to be related to forming a gate structure. See Jeng, column 3, lines 10-28; column 4, lines 18-27; and FIG. 2.

Because the Jeng reference fails to supply the missing teachings of Puchner and Cabral, no *prima facie* case of obviousness has been made. For at least this reason, applicant requests that the rejection be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully requests reconsideration of this application and the timely allowance of the pending claims.

In the event that the Examiner determines that any outstanding issues remain that would prevent an immediate allowance of this application, it is requested that the Examiner contact applicants' undersigned representative, Matthew Whipple, at (703) 917-0000, Ext. 103, in order that the issues be quickly resolved and the case moved to allowance.

Please grant any extensions of time required to enter this response and charge any additional required fees to Texas Instruments' Deposit Account 20-0668.

Respectfully submitted,

Dated: June 21, 2007

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